

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	10550323
Filing Date	2005-09-23
First Named Inventor	Roger D. Chamberlain
Art Unit	2494 2162
Examiner Name	Hennings, Matthew T JBF
Attorney Docket Number	53047-57370

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	4	7408932		2008-08-05	Kounavis et al.	
	5	7411957		2008-08-12	Stacy et al.	
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	2	WARD ET AL., "Dynamically Reconfigurable Computing: A Novel Computation Technology with Potential to Improve National Security Capabilities", May 15, 2003, A White Paper Prepared by Star Bridge Systems, Inc. [retrieved 2006-12-12]. Retrieved from the Internet: <URL: http://www.starbridgesystems.com/resources/whitepapers/Dynamically%20Reconfigurable%20Computing.pdf > .All Pages.	<input type="checkbox"/>
	3	WEST ET AL., "An FPGA-Based Search Engine for Unstructured Database", Proc. of 2nd Workshop on Application Specific Processors, December 2003, San Diego, CA .All Pages .09/01/2006 .	<input type="checkbox"/>
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	5	Written Opinion for PCT/US2004/016398 dated June 9, 2005 .All Pages .	<input type="checkbox"/>
	6	ZIV ET AL., " A Universal Algorithm for Sequential Data Compression", IEEE Trans. Inform. Theory, IT-23(3): 337-343 (1997)	<input type="checkbox"/>
	7	ZIV ET AL., "Compression of Individual Sequence via Variable-Rate Coding", IEEE Transactions on Information Theory, Sept. 1978, pp. 530-536, Vol. IT-24, No. 5, Institute of Electrical and Electronics Engineers, Washington, DC, USA	<input type="checkbox"/>

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